Amendments To The Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 **(amended)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, ~~**the current being less than or equal to a maximum magnitude I_{M1}**~~ **said current having a magnitude of substantially I_{M1} to represent a first data state and a magnitude of substantially zero to represent a second data state**;

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, ~~**the current being less than or equal to a maximum magnitude I_{M2}**~~ **said current having a magnitude of substantially zero to represent the first data state and a magnitude of substantially I_{M2} to represent the second data state**;

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1} ;

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2} ; [[**and**]]

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier**; and**

a read circuit to read the data states of the first and second plurality of memory cells, said read circuit providing an activation signal to the read-select input of only one of the first plurality or second plurality of memory cells at a time, said read circuit further providing an enable signal to the enable input of the first reference current circuit when said activation signal is provided to a memory cell of the first plurality of memory cells, and providing an enable signal to the enable input of the second reference current circuit when said activation signal is provided to a memory cell of the second plurality of memory cells.

Claim 2 **(canceled)** ~~**The memory of Claim 1, wherein the first reference current circuit is activated when any one of the read-select inputs of the first plurality of memory cells is activated, and wherein the second reference current circuit is activated when any one of the read-select inputs of the second plurality of memory cells is activated.**~~

Claim 3 **(amended)**: The memory device of Claim 1 ~~**further comprising**~~ **wherein the read circuit comprises**:

a plurality of first read word lines, each first read word line being coupled to the read-select input of a respective one of the first plurality of memory cells;

a plurality of second read word lines, each second read word line being coupled to the read-select input of a respective one of the second plurality of memory cells; and

a read control/decoder that is responsive to a set of address bits and that has a plurality of control outputs, each first read word line being coupled to a respective one of the control outputs, each second read word line being coupled to a respective one of the control outputs, the enable input of the first ~~**current reference cell**~~ **reference current circuit** being coupled to a respective one of the control outputs, and the enable input of the second ~~**current reference cell**~~ **reference current circuit** being coupled to a respective one of the control outputs, said read control/decoder generating an activation signal to the first reference current circuit when it generates an activation signal to any one of the first read word lines, and further generating an activation signal to the

second reference current circuit when it generates an activation signal to any one of the second read word lines.

Claim 4 **(canceled)**: ~~**The memory of Claim 1, wherein the data states of the first and second plurality of memory cells are selectively sensed by said current sense amplifier during a read operation, and wherein the read-select input of only one of the memory cells is activated during the read operation**~~.

Claim 5 **(amended)**: The memory of Claim 1, ~~**wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and**~~ wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.25 \cdot I_{M1}$ and approximately $0.75 \cdot I_{M1}$.

Claim 6 **(amended)**: The memory of Claim 5, ~~**wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and**~~ wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.25 \cdot I_{M2}$ and approximately $0.75 \cdot I_{M2}$.

Claim 7 **(amended)**: The memory of Claim 1, ~~**wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and**~~ wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.25 \cdot I_{M2}$ and approximately $0.75 \cdot I_{M2}$.

Claim 8 **(amended)**: The memory of Claim 1, ~~**wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data**~~

~~state, and~~ wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.3 \cdot I_{M1}$ and approximately $0.6 \cdot I_{M1}$.

Claim 9 **(amended)**: The memory of Claim 1, ~~wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and~~ wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.35 \cdot I_{M1}$ and approximately $0.45 \cdot I_{M1}$.

Claim 10 **(amended)**: The memory of Claim 9, ~~wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and~~ wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

Claim 11 **(amended)**: The memory of Claim 1, ~~wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and~~ wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

Claim 12 **(amended)**: The memory of Claim 1, ~~wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and~~ wherein the magnitude of current I_{R1} generated by the first reference current circuit is equal to or less than approximately $0.5 \cdot I_{M1}$.

Claim 13 **(original)**: The memory of Claim 1, wherein each of the magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 100 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 14 **(amended)**: The memory of Claim 1, wherein each of **the** magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 500 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 15 **(canceled)**: ~~**The memory of Claim 1, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein each memory cell of the second plurality of memory cells generates a current of substantially zero magnitude to represent the first data state and a current having a magnitude of substantially I_{M2} to represent the second data state.**~~

Claim 16 **(original)**: The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.2 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 17 **(original)**: The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.5 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 18 **(original)**: The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $[1.9 - N_W/160] \cdot L_{MIN}$, where N_W is the number of word lines which are spanned by one of the bit lines, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 19 **(amended)**: The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has **a** W/L ratio of channel

width to channel length, and wherein the W/L ratio is less than approximately $3.4 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 20 **(amended)**: The memory of Claim 1, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has **a** W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $1.7 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claims 21 – 37 **(canceled)**

Claim 38 **(amended)**: A method of reading data stored in a memory, the memory having a first plurality of memory cells and a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, each memory cell of the first plurality of memory cells having its read output coupled to a first bit line and generating a current at its read output that has a magnitude less than or equal to a maximum magnitude I_{M1}, each memory cell of the second plurality of memory cells having its read output coupled to a second bit line and generating a current at its read output that has a magnitude less than or equal to a maximum magnitude I_{M2}, said method comprising the steps of:

(a) selecting a memory cell in one of the first and second plurality of memory cells by providing a signal to its read-select ~~**input,**~~ **input such that the selected memory cell generates a current having a magnitude of substantially I_{M1} to represent a first data state and a magnitude of substantially zero to represent a second data state when the selected memory cell is from the first plurality of memory cells, and such that the selected memory cell**

generates a current having a magnitude of substantially zero to represent the first data state and a magnitude of substantially I_{M2} to represent the second data state when the selected memory cell is from the second plurality of memory cells;

(b) coupling a current I_{R1} to the second bit line when step (a) selects a memory cell of the first plurality of memory cells, the magnitude of current I_{R1} ~~being less than or equal to $0.7 \cdot I_{M1}$~~ **ranging between approximately $0.25 \cdot I_{M1}$ and approximately $0.75 \cdot I_{M1}$;**

(c) coupling a current I_{R2} to the first bit line when step (a) selects a memory cell of the second plurality of memory cells, the magnitude of current I_{R2} ~~being less than or equal to $0.7 \cdot I_{M2}$~~ **ranging between approximately $0.25 \cdot I_{M2}$ and approximately $0.75 \cdot I_{M2}$**; and

(d) sensing a difference in the currents on the first and second bit lines with a current sense amplifier.

Claim 39 **(original)**: The method of Claim 38, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} ranges between approximately $0.3 \cdot I_{M1}$ and approximately $0.6 \cdot I_{M1}$.

Claim 40 **(original)**: The method of Claim 39, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} ranges between approximately $0.3 \cdot I_{M2}$ and approximately $0.6 \cdot I_{M2}$.

Claim 41 **(new)**: The method of Claim 38, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} ranges between approximately $0.35 \cdot I_{M1}$ and approximately $0.45 \cdot I_{M1}$.

Claim 42 **(new)**: The method of Claim 41, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data

state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

Claim 43 **(new)**: The method of Claim 38, wherein each of the magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 100 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 44 **(new)**: The method of Claim 38, wherein each of magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 500 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 45 **(new)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1} ;

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2} ;

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2} ; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier; and

wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.25 \cdot I_{M1}$ and approximately $0.75 \cdot I_{M1}$.

Claim 46 **(new)**: The memory of Claim 45, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.3 \cdot I_{M1}$ and approximately $0.6 \cdot I_{M1}$.

Claim 47 **(new)**: The memory of Claim 45, wherein each memory cell of the first plurality of memory cells generates a current having a magnitude of substantially I_{M1} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R1} generated by the first reference current circuit ranges between approximately $0.35 \cdot I_{M1}$ and approximately $0.45 \cdot I_{M1}$.

Claim 48 **(new)**: The memory of Claim 47, wherein each memory cell of the second plurality of memory cells generates a current having a magnitude of substantially I_{M2} to represent a first data state and a current of substantially zero magnitude to represent a second data state, and wherein the magnitude of current I_{R2} generated by the second reference current circuit ranges between approximately $0.35 \cdot I_{M2}$ and approximately $0.45 \cdot I_{M2}$.

Claim 49 **(new)**: The memory of Claim 45, wherein each of the magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 100 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 50 **(new)**: The memory of Claim 45, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.2 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 51 **(new)**: The memory of Claim 45, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $[1.9 - N_W/160] \cdot L_{MIN}$, where N_W is the number of word lines which are spanned by one of the bit lines, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 52 **(new)**: The memory of Claim 45, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $3.4 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 53 **(new)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1};

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2};

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2} ; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier; and

wherein each of the magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 100 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 54 **(new)**: The memory of Claim 53, wherein each of magnitudes of I_{M1}, I_{M2}, I_{R1}, and I_{R2} is at least 500 times larger than the maximum expected leakage current on the bit line to which the current is coupled.

Claim 55 **(new)**: The memory of Claim 53, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.2 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 56 **(new)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1};

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2};

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2}; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier; and

wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $1.2 \cdot L_{MIN}$, where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 57 **(new)**: The memory of Claim 56, wherein the selection transistor has a channel length of at least $1.5 \cdot L_{MIN}$.

Claim 58 **(new)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1};

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2};

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2}; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier; and

wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has a channel length of at least $[1.9 - N_W/160] \cdot L_{MIN}$, where N_W is the number of word lines which are spanned by one of the bit lines, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 59 **(new)**: A memory device comprising:

a first plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M1};

a second plurality of memory cells, each memory cell having a read-select input and a read output, each memory cell generating a current at its read output that is representative of a data

value stored by the cell when the read-select input of the memory cell is activated, the current being less than or equal to a maximum magnitude I_{M2};

a first bit line coupled to the read outputs of the first plurality of memory cells;

a second bit line coupled to the read outputs of the second plurality of memory cells;

a first reference current circuit having an enable input and an output, the output being coupled to the second bit line, the first reference current circuit generating a first reference current I_{R1} at its output when its enable input is activated, the first reference current I_{R1} having a magnitude that is less than I_{M1};

a second reference current circuit having an enable input and an output, the output being coupled to the first bit line, the second reference current circuit generating a second reference current I_{R2} at its output when its input is activated, the second reference current I_{R2} having a magnitude that is less than I_{M2}; and

a current sense amplifier having a first input coupled to the first bit line, a second input coupled to the second bit line, and an output generating a signal representative of the difference in currents presented at the inputs of the differential current sense amplifier; and

wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $3.4 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.

Claim 60 **(new):** The memory of Claim 59, wherein each memory cell comprises a selection transistor coupled to its read output, wherein the selection transistor has W/L ratio of channel width to channel length, and wherein the W/L ratio is less than approximately $1.7 \cdot W_{MIN}/L_{MIN}$, where W_{MIN} is the minimum transistor channel width permitted for the transistor in the integrated-circuit technology used to construct the memory device, and where L_{MIN} is the minimum transistor channel length permitted for the transistor in the integrated-circuit technology used to construct the memory device.